

RMI Alchemy™ Au1200™ Processor Portable Media Player (PMP) Reference Design Schematics

IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in yellow are notes of caution.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

3) DESIGN NOTES in red are critical, and must be understood and followed.

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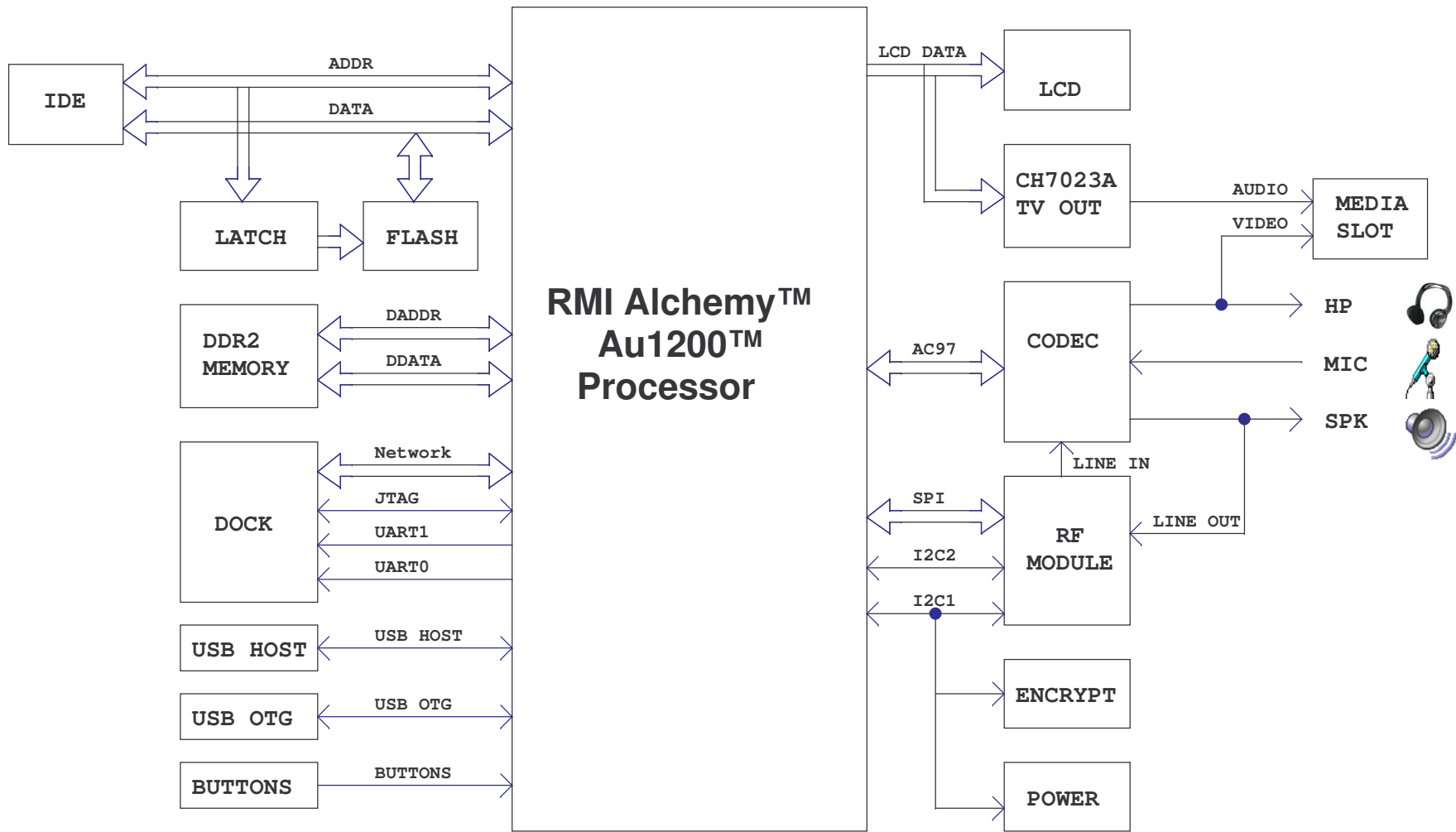
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INITIAL POWER UP SEQUENCE:

- 1) SWITCH SHDN LOW TO RUN SMB122 CHIP
- 2) VDDX AND VDDY POWER UP
- 3) VDDX_OK FROM HEALTHY SIGNAL GOES ACTIVE
- 4) PWR_EN GOES ACTIVE BY HOST CPU
- 5) VDDI POWERS UP
- 6) AU_RESET IS RELEASED AFTER DELAY
- 7) SYSTEM BEGINS TO RUN
- 8) 5V IS POWERED UP BY I2C COMMAND
- 9) 2.5V IS POWERED UP BY I2C COMMAND
- 10) LED BACKLIGHT IS POWERED UP BY I2C COMMAND

SLEEP SEQUENCE:

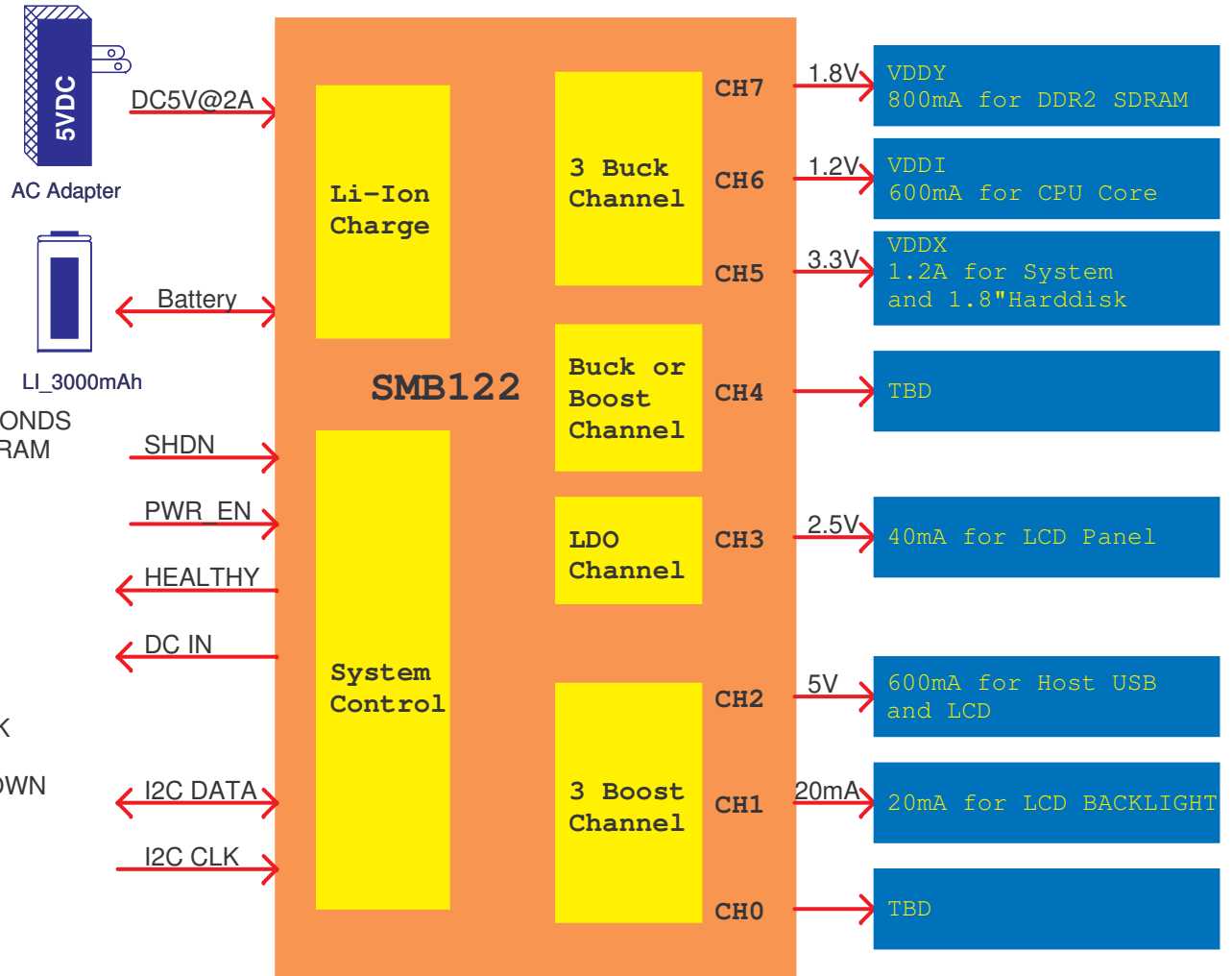
- 1) PRESS WAKE/SLEEP BUTTON FOR MORE THAN 3 SECONDS
- 2) HOST PREPARES FOR SLEEP INCLUDING IDE AND SDRAM
- 3) HOST CLOSES LED BACKLIGHT VIA I2C COMMAND
- 4) HOST CLOSES 5V VIA I2C COMMAND
- 5) HOST CLOSES 2.5V VIA I2C COMMAND
- 6) HOST DISENABLES PWR_EN
- 7) VDDI POWERS DOWN

SHUT DOWN SEQUENCE:

- 1) OPERATE AS SLEEP SEQUENCE
- 2) WAIT FOR SEVERAL SECONDS TILL LCD TURNS BLACK
- 3) SWITCH SHDN HIGHT
- 4) ALL POWER INCLUDING VDDY AND VDDX POWERS DOWN

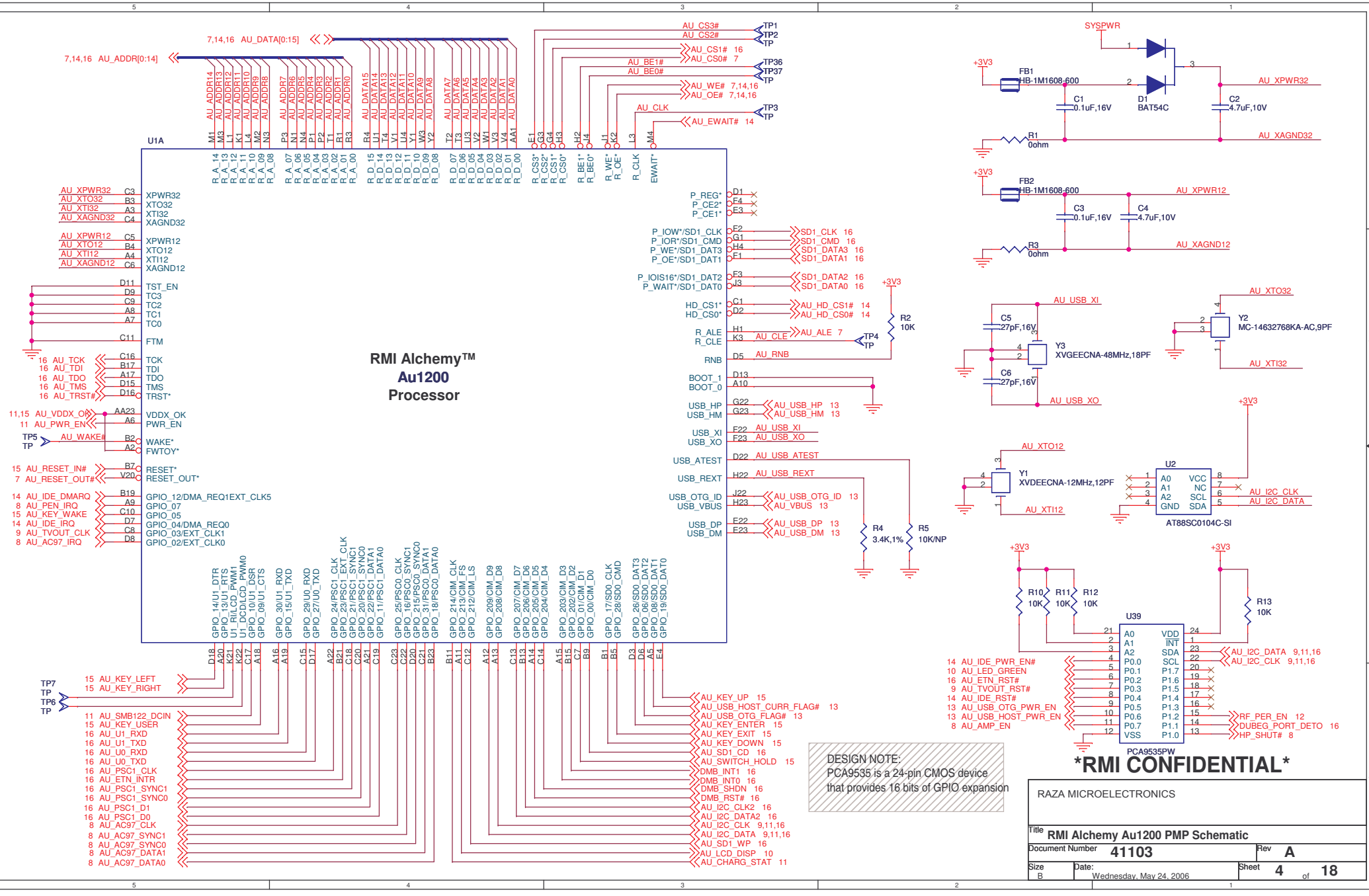
WAKE UP FROM SLEEP SEQUENCE:

- 1) TOY IS ACTIVATED OR PRESS WAKE/SLEEP BUTTON
- 2) HOST ASSERTS PWR_EN
- 3) VDDI POWERS UP
- 4) DO SOME NECESSARY SOFTWARE OPERATION
- 5) RESUME 2.5V VIA I2C COMMAND
- 6) RESUME 5V VIA I2C COMMAND
- 7) RESUME LED BACKLIGHT VIA I2C COMMAND



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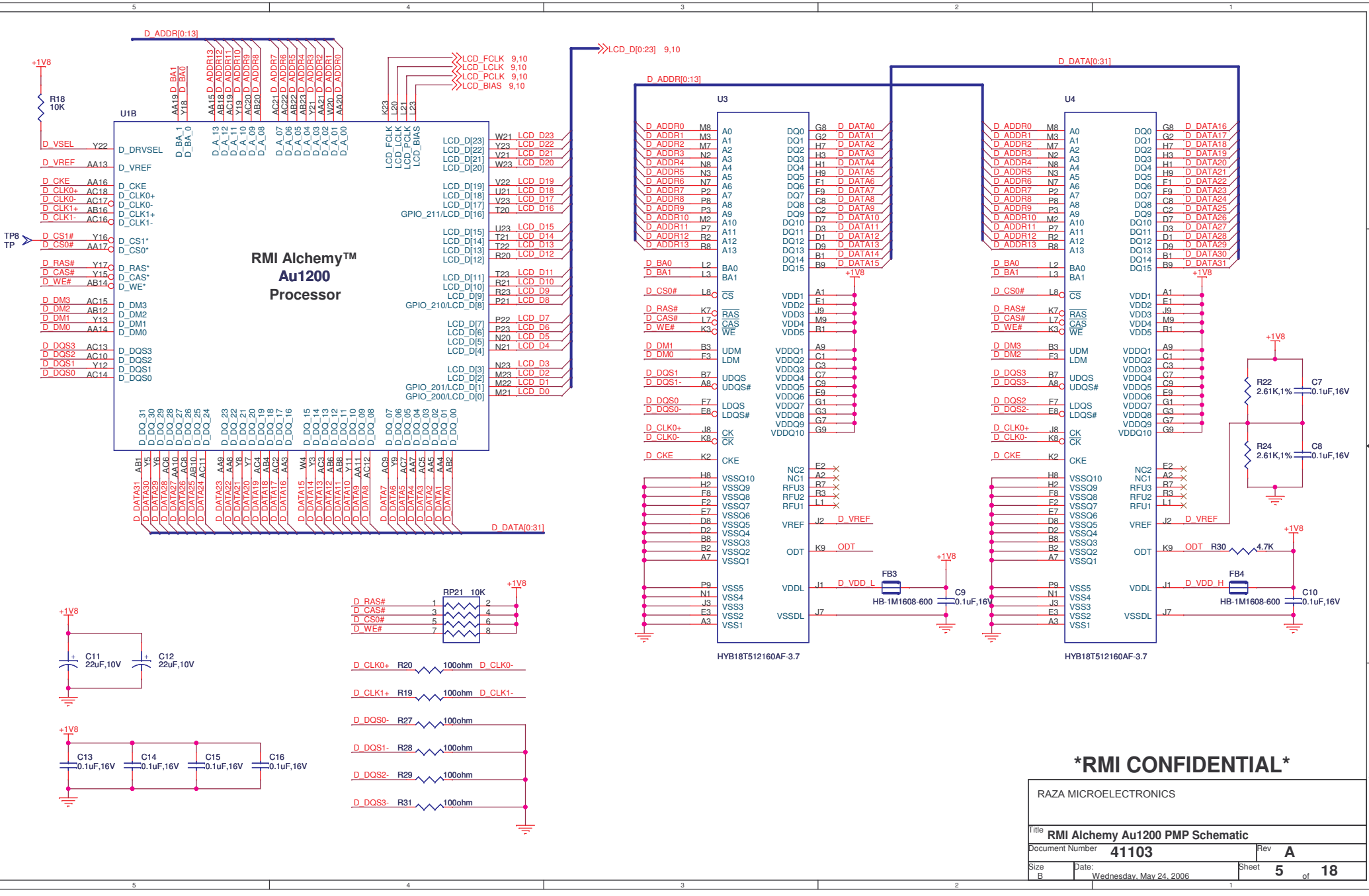


**RMI Alchemy™
Au1200
Processor**

DESIGN NOTE:
PCA9535 is a 24-pin CMOS device
that provides 16 bits of GPIO expansion

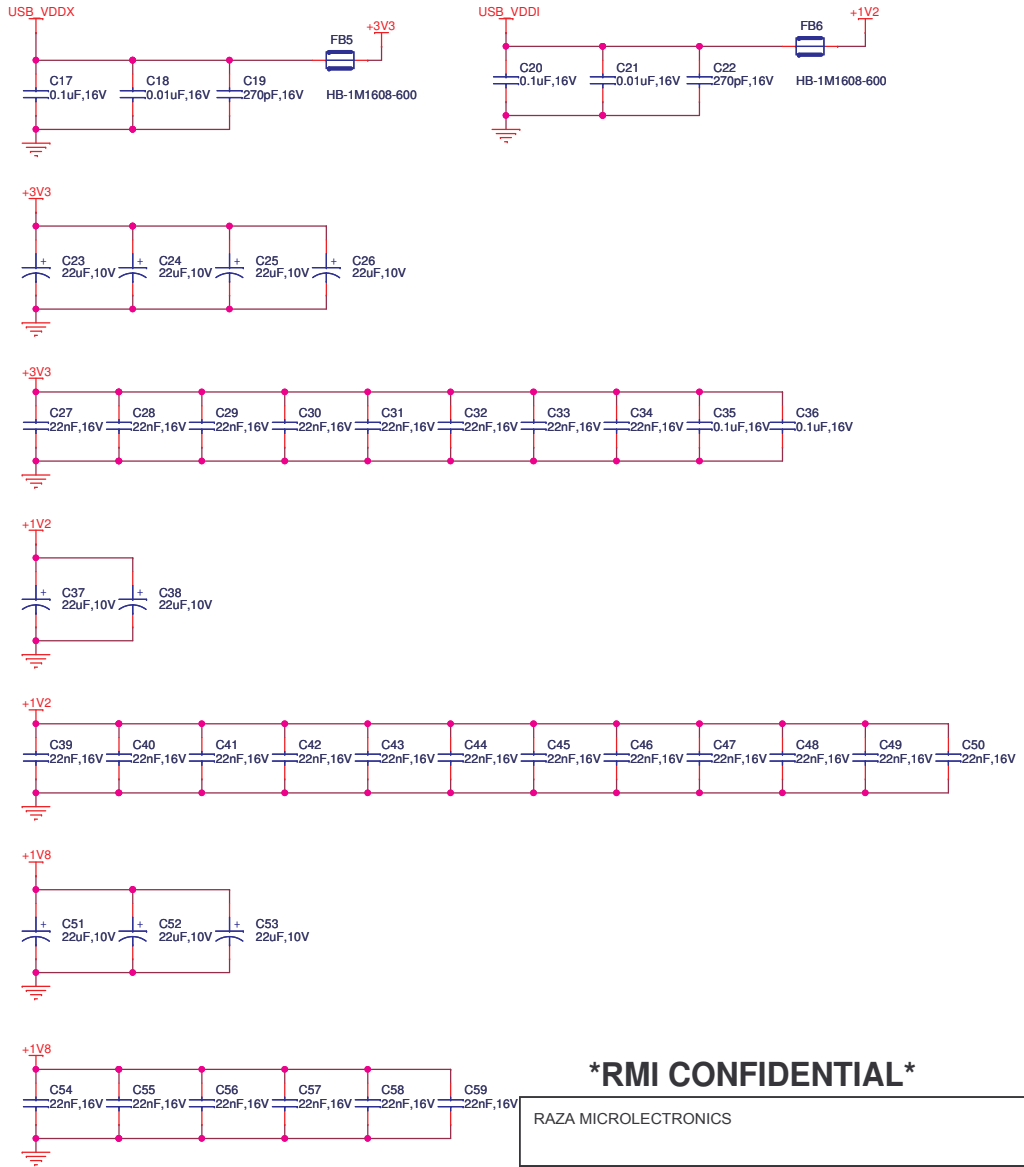
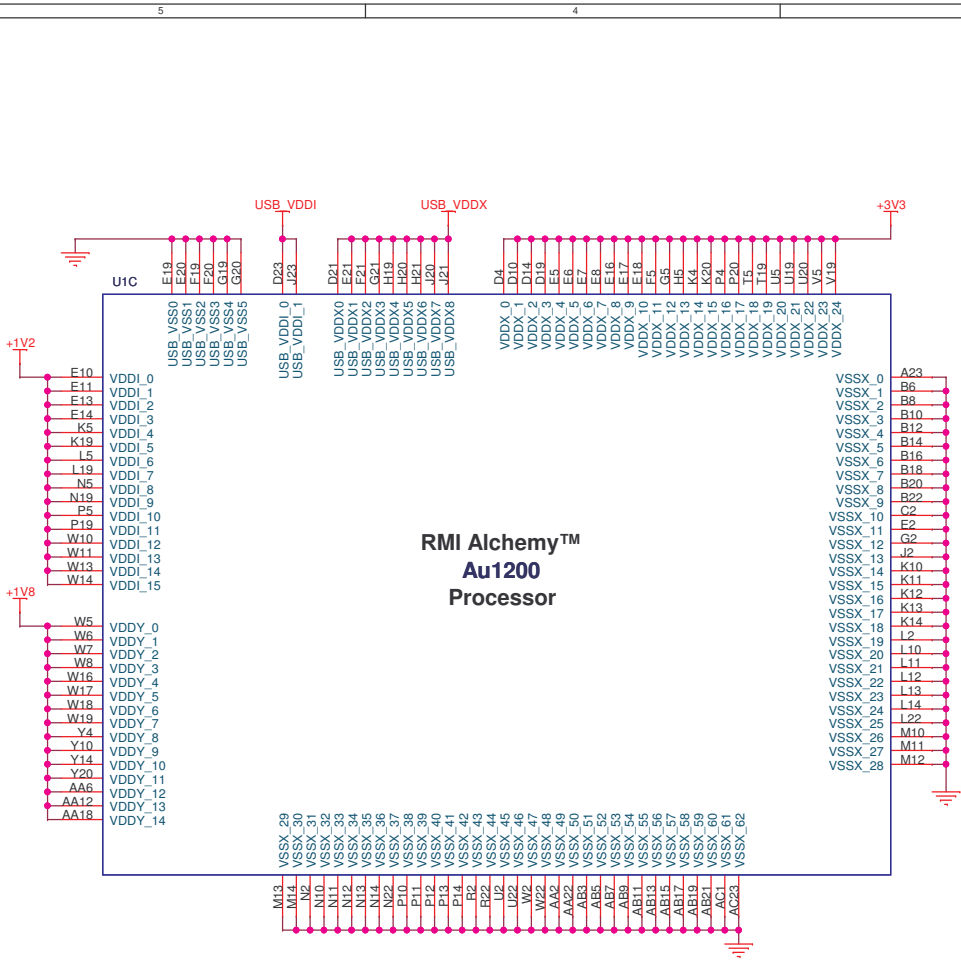
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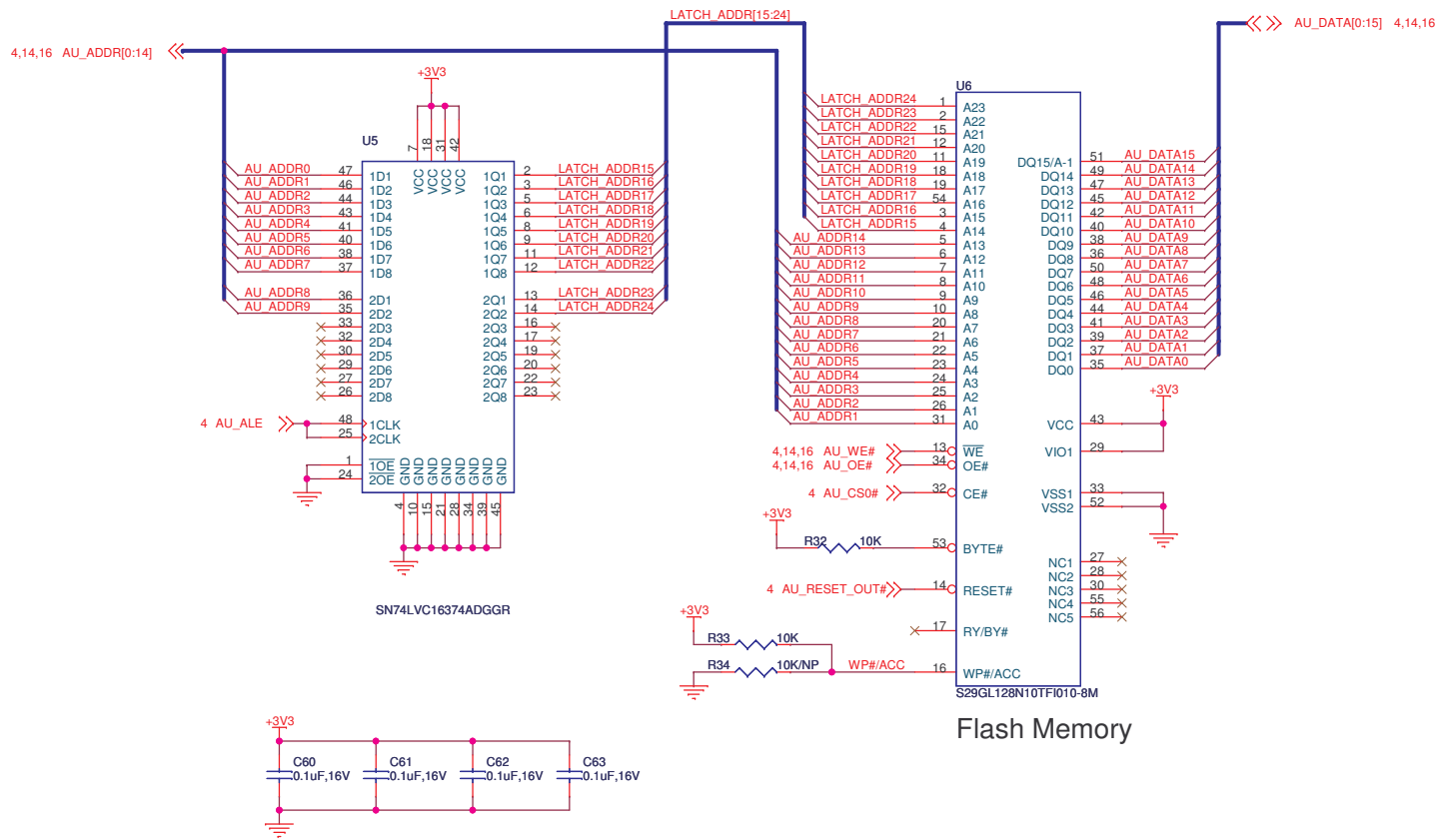
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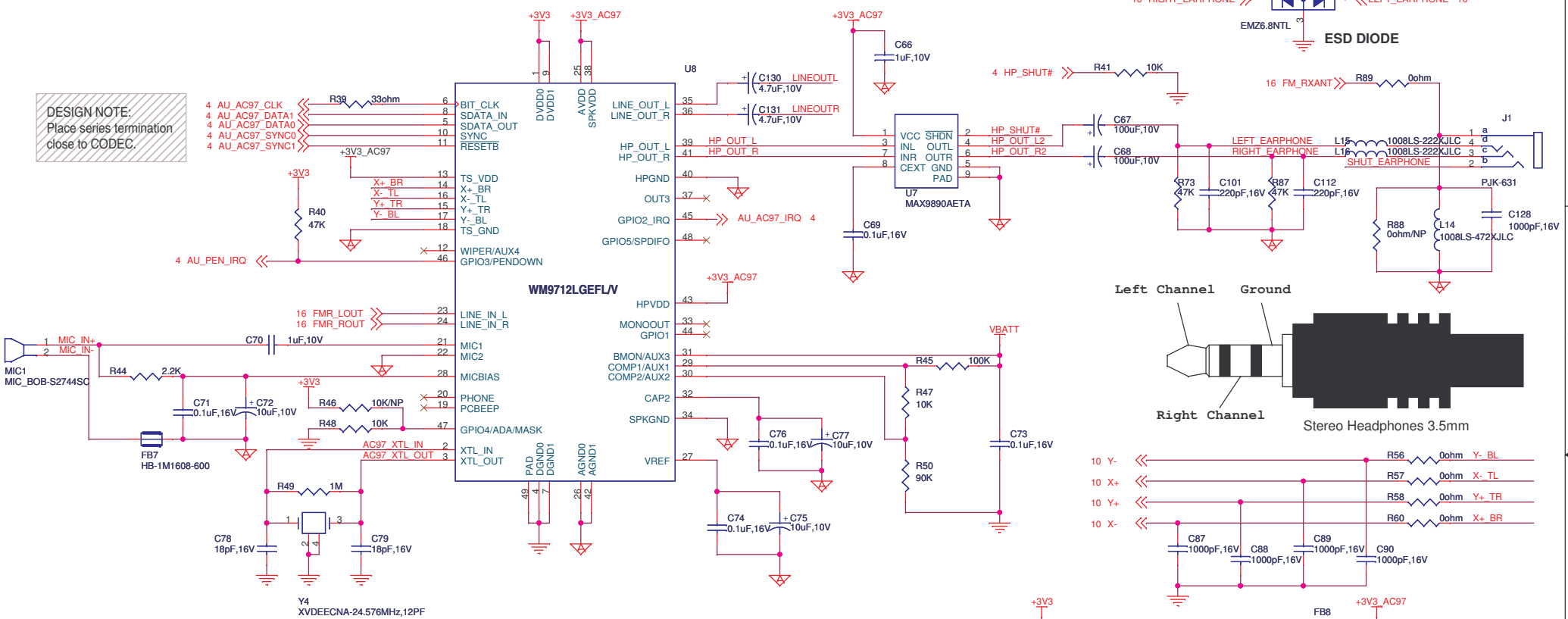


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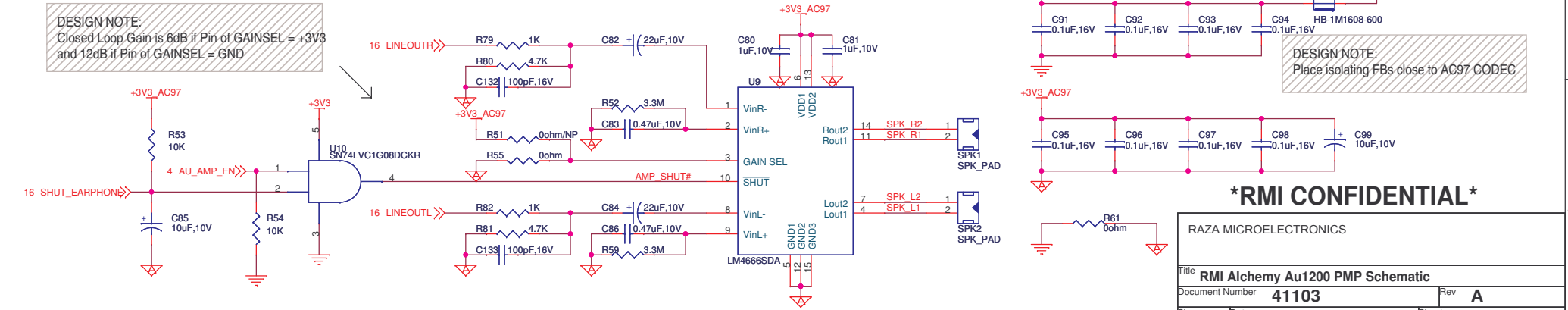
DESIGN NOTE:
Place series termination close to CODEC.

- 4 AU_AC97_CLK
- 4 AU_AC97_DATA1
- 4 AU_AC97_DATA0
- 4 AU_AC97_SYNC0
- 4 AU_AC97_SYNC1

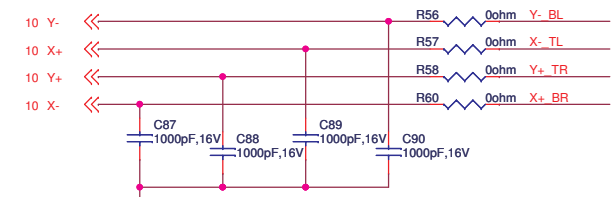
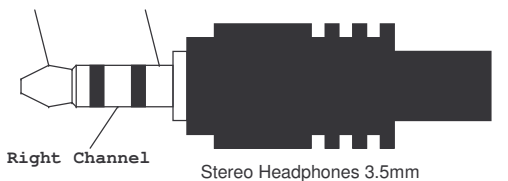
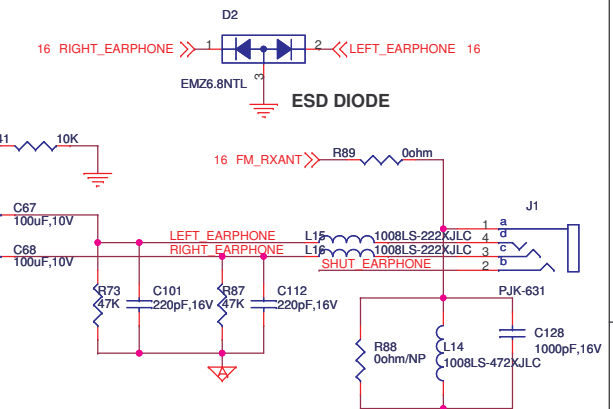


Y4 XVDEECNA-24.576MHz,12PF

DESIGN NOTE:
Closed Loop Gain is 6dB if Pin of GAINSEL = +3V3 and 12dB if Pin of GAINSEL = GND

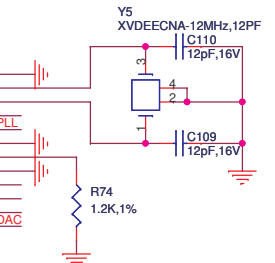
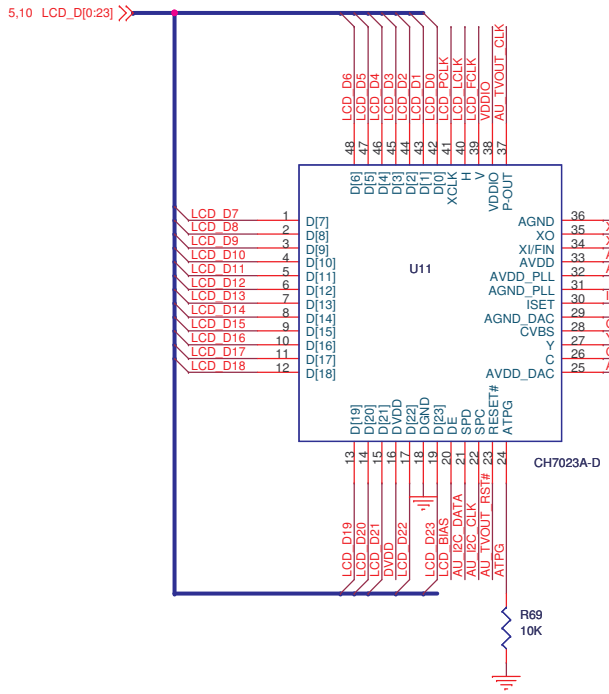


DESIGN NOTE:
Place isolating FBs close to AC97 CODEC

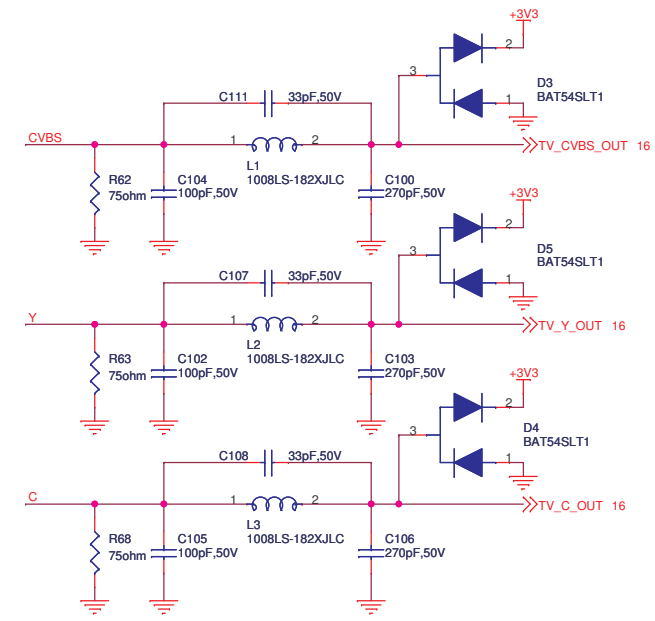


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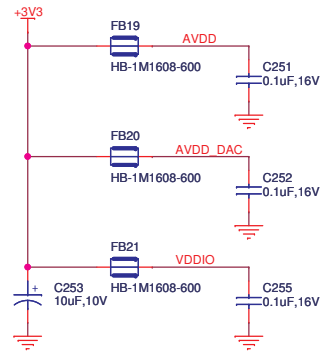
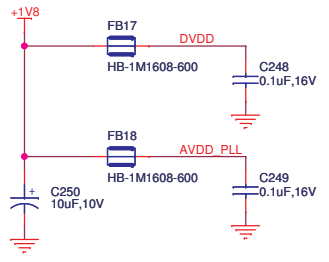
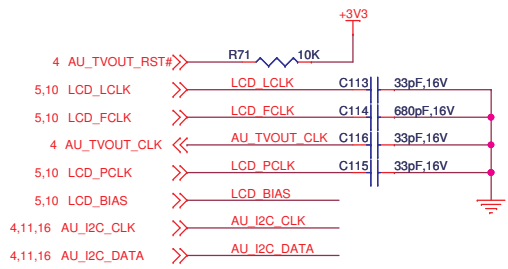
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DESIGN NOTE:
 This pin(Pin 30) sets the DAC current. A 1.2k ohm, 1% tolerance resistor should be connected between this pin and AGND_DAC (pin 39) using short and wide traces.



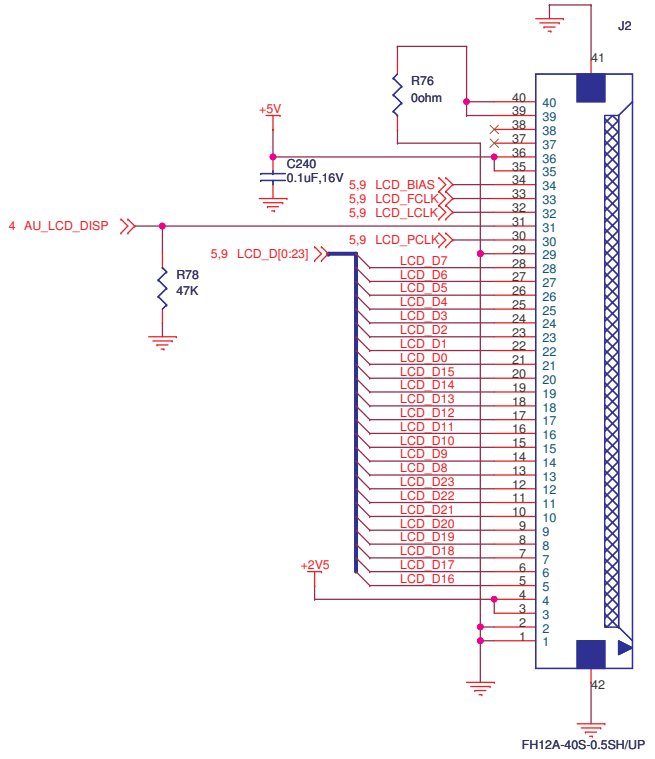
DESIGN NOTE:
 Place all these passive components close to slot



DESIGN NOTE:
 Place all these FBs close to U11

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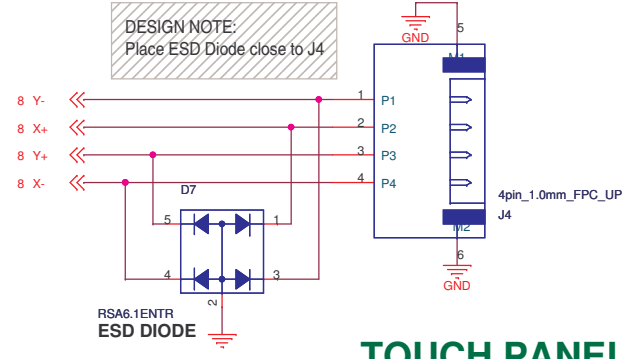
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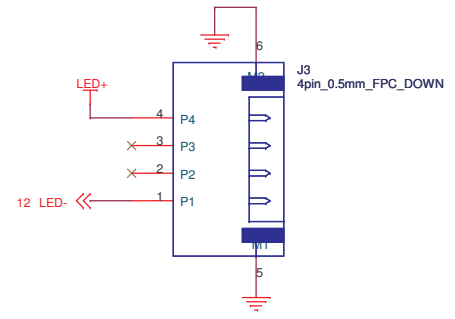
TFT LCD

DESIGN NOTE: LCD SIGNALS

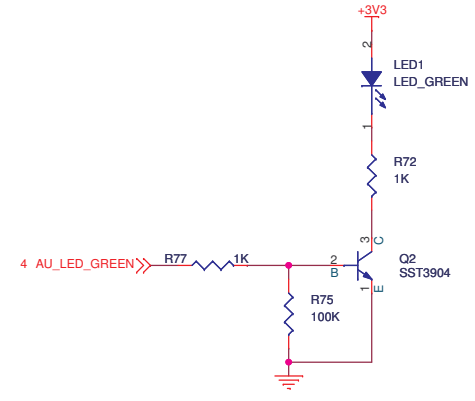
LCD_D[0]	- B0
LCD_D[1]	- B1
LCD_D[2]	- B0 - B2
LCD_D[3]	- B1 - B3
LCD_D[4]	- B2 - B4
LCD_D[5]	- B3 - B5
LCD_D[6]	- B4 - B6
LCD_D[7]	- B5 - B7
LCD_D[8]	- G0
LCD_D[9]	- G1
LCD_D[10]	- G0 - G2
LCD_D[11]	- G1 - G3
LCD_D[12]	- G2 - G4
LCD_D[13]	- G3 - G5
LCD_D[14]	- G4 - G6
LCD_D[15]	- G5 - G7
LCD_D[16]	- R0
LCD_D[17]	- R1
LCD_D[18]	- R0 - R2
LCD_D[19]	- R1 - R3
LCD_D[20]	- R2 - R4
LCD_D[21]	- R3 - R5
LCD_D[22]	- R4 - R6
LCD_D[23]	- R5 - R7



TOUCH PANEL

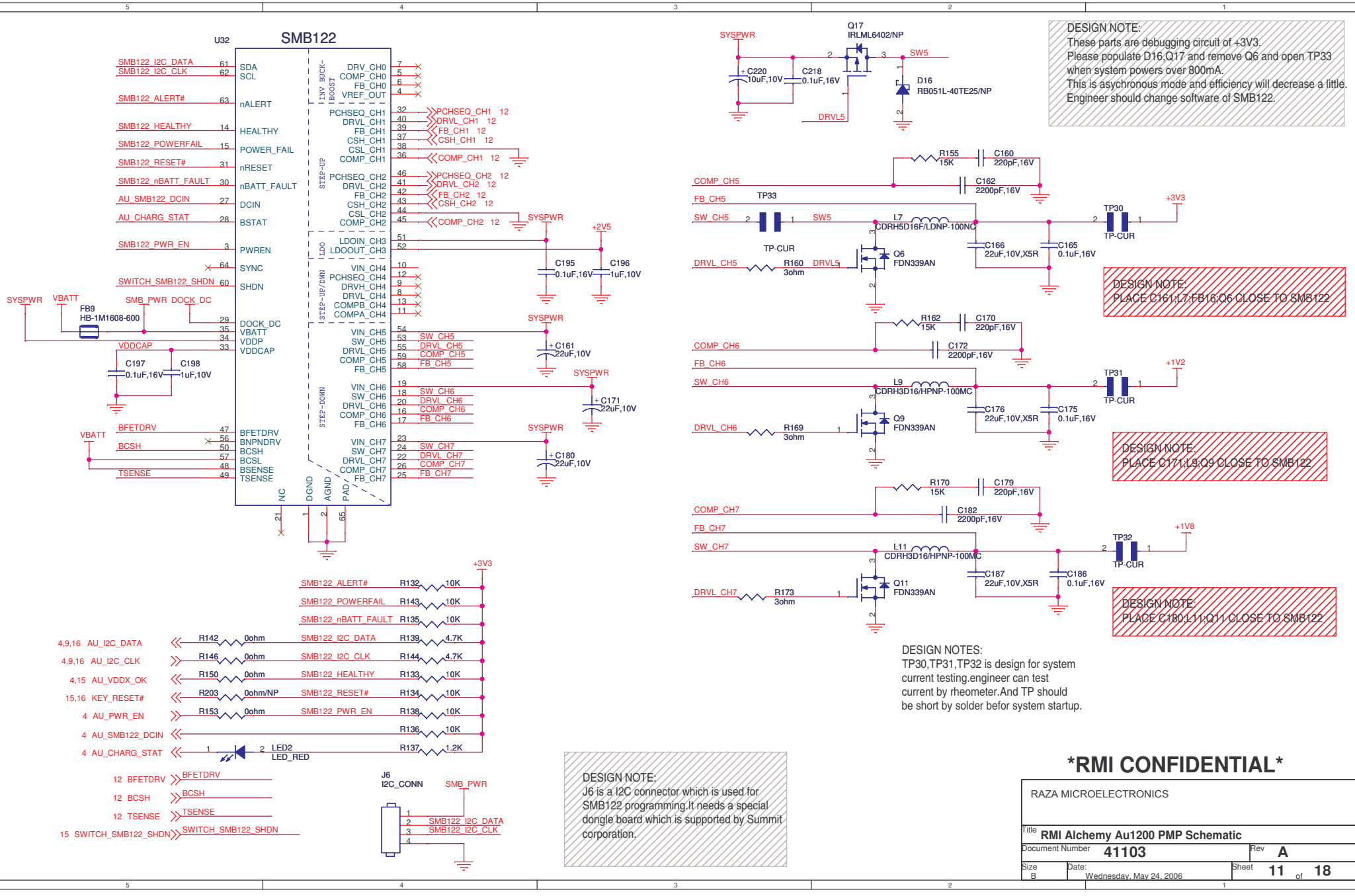


BACKLIGHT



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DESIGN NOTE:
 These parts are debugging circuit of +3V3.
 Please populate D16, Q17 and remove Q6 and open TP33
 when system powers over 800mA.
 This is asynchronous mode and efficiency will decrease a little.
 Engineer should change software of SMB122.

DESIGN NOTE:
 PLACE C161, L7, FB16, Q6 CLOSE TO SMB122

DESIGN NOTE:
 PLACE C171, L9, Q9 CLOSE TO SMB122

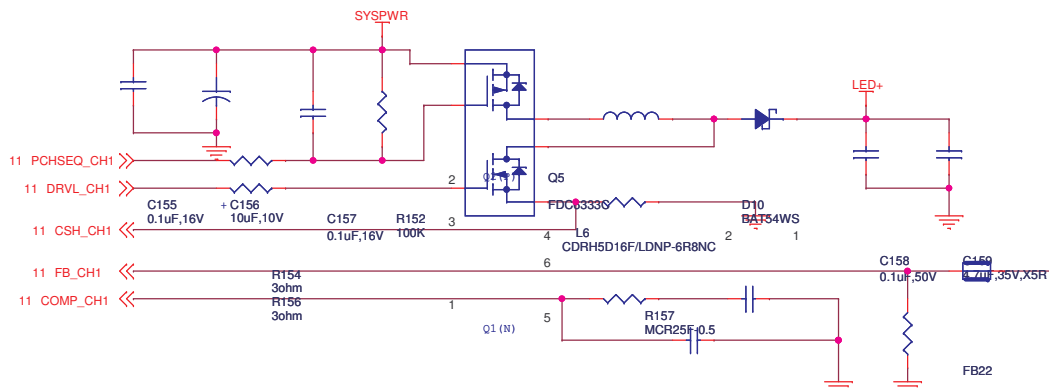
DESIGN NOTE:
 PLACE C180, L11, Q11 CLOSE TO SMB122

DESIGN NOTES:
 TP30, TP31, TP32 is design for system
 current testing. engineer can test
 current by rheometer. And TP should
 be short by solder before system startup.

DESIGN NOTE:
 J6 is a I2C connector which is used for
 SMB122 programming. It needs a special
 dongle board which is supported by Summit
 corporation.

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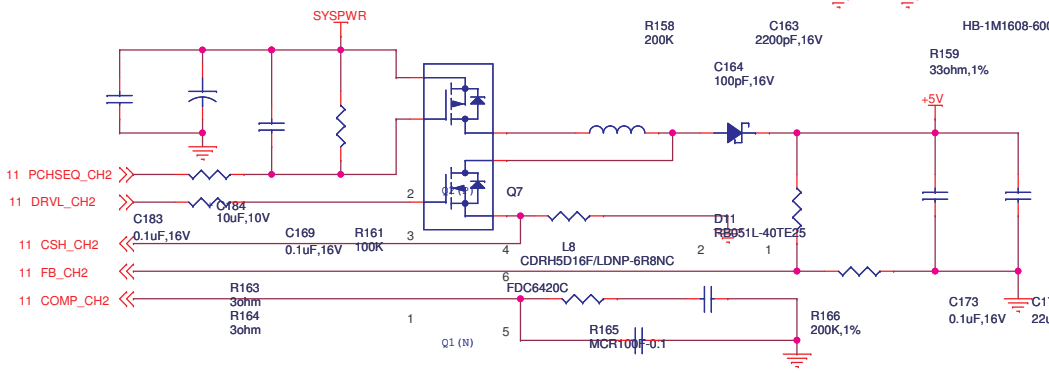


DESIGN NOTE:
PLACE INPUT CAPACITOR CLOSE
TO CHANNEL 1 INPUT PORT

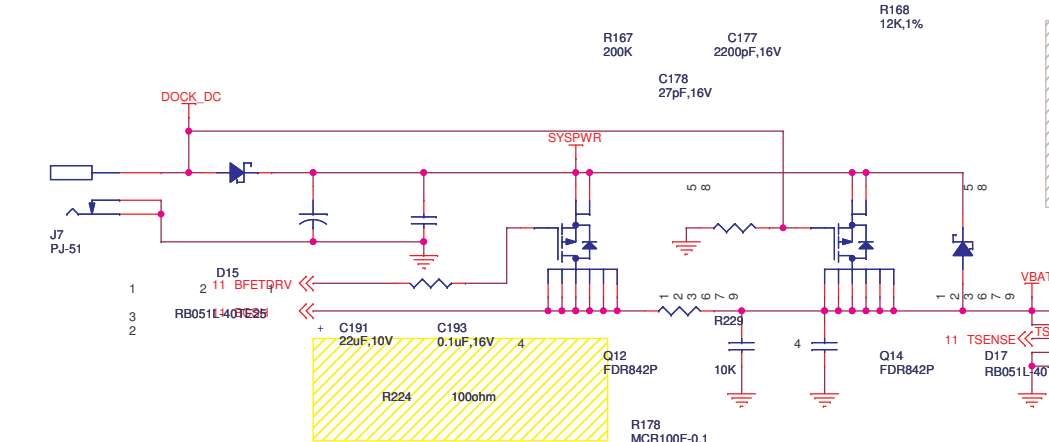
DESIGN NOTE:
PLACE Q5;L6;D10;R157;C159
TOGETHER AS CLOSE AS POSSIBLE



DESIGN NOTE:
PLACE INPUT CAPACITOR CLOSE
TO CHANNEL 2 INPUT PORT

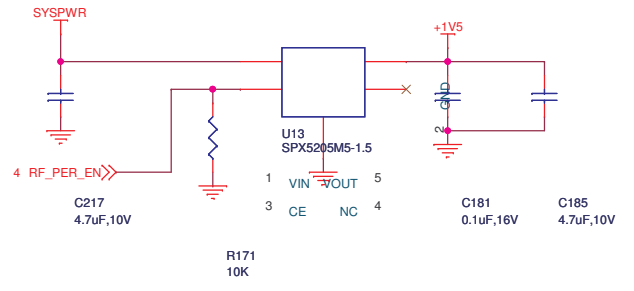


DESIGN NOTE:
PLACE Q7;L8;D11;R165;C174
TOGETHER AS CLOSE AS POSSIBLE



DESIGN NOTE:
When the adapter is present Q14 is turned off
and the adapter powers the system and Q12
charges the battery. When the adapter is not
present, Q12 is turned off and Q14 turns on
to run the system from the battery.

DESIGN NOTE:
Please refer to datasheet of FDR842P
to get detail information for layout
recomendation

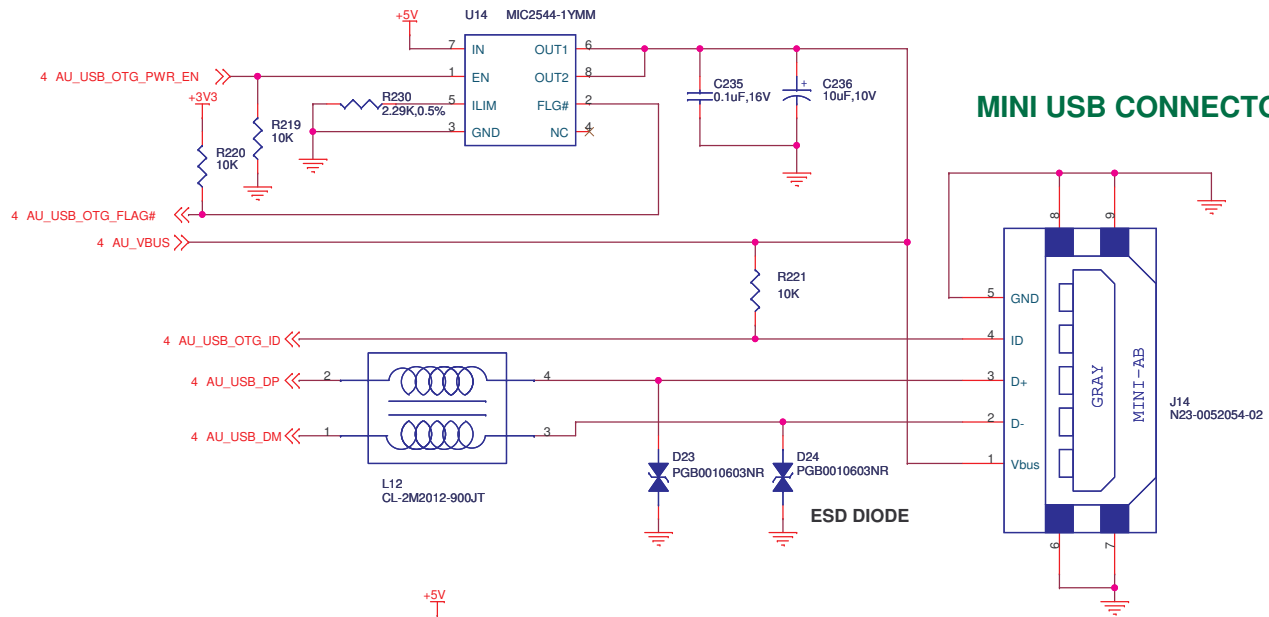


R171
10K

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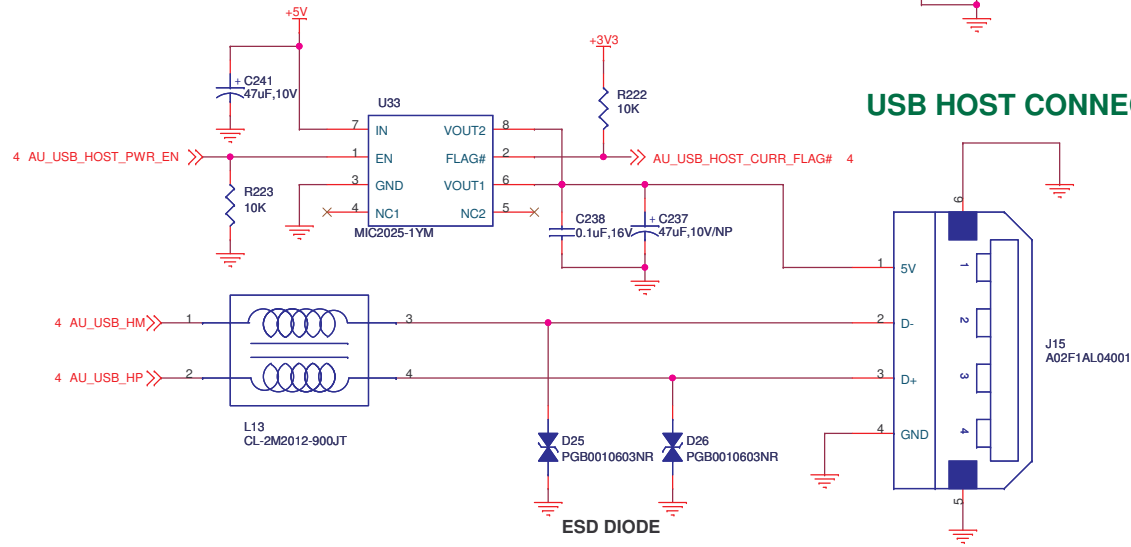
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A1250WV-S-5P



MINI USB CONNECTOR

DESIGN NOTE:
Current limit is set to 100mA

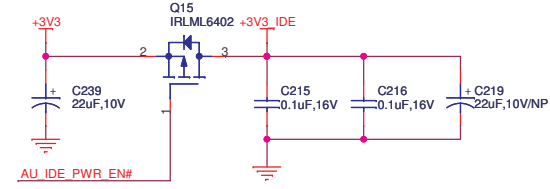
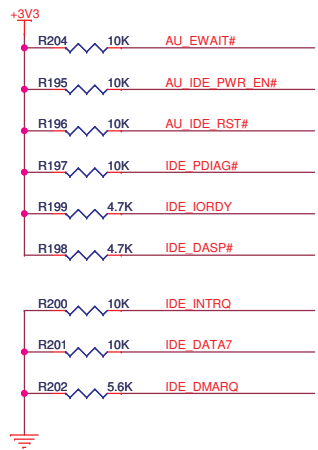
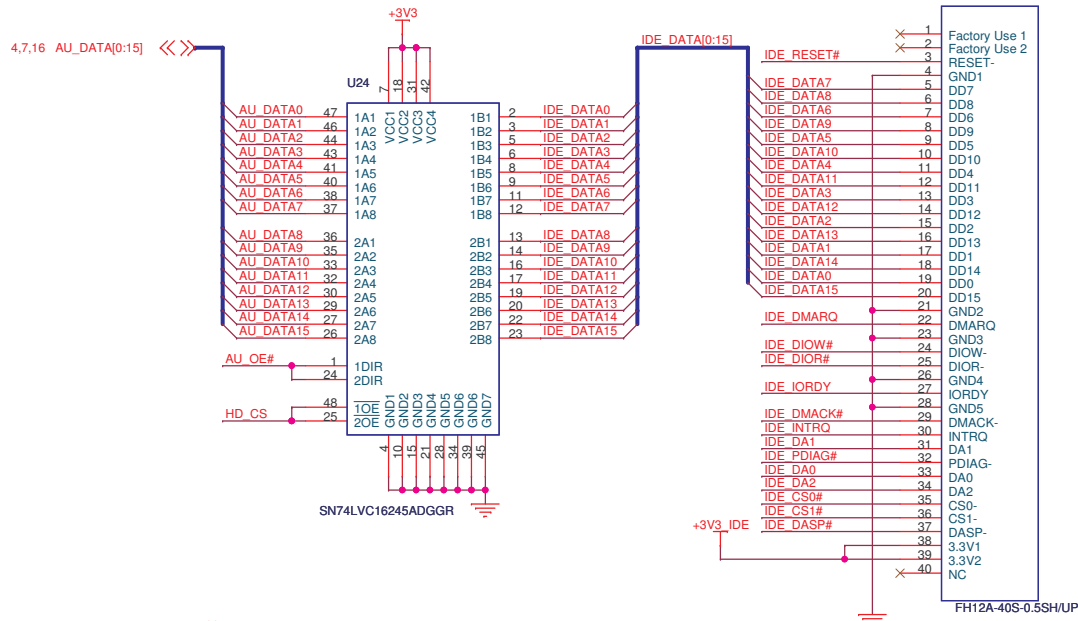


USB HOST CONNECTOR

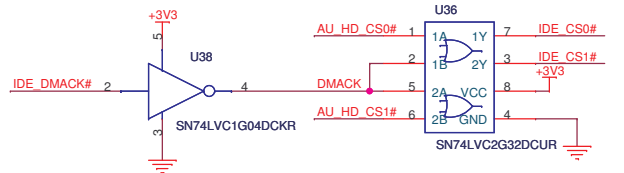
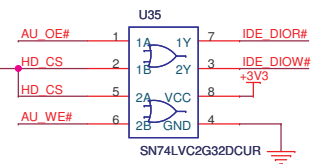
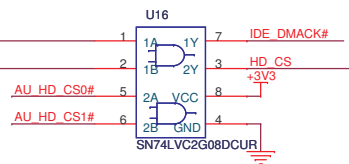
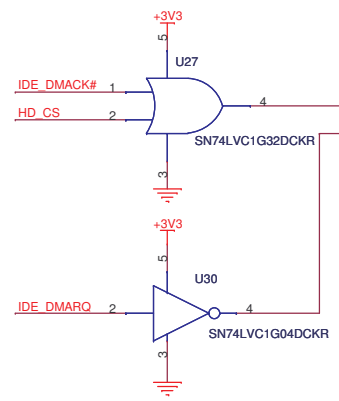
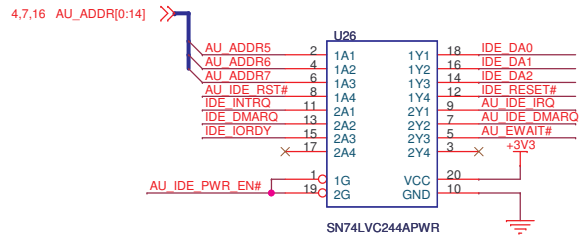
DESIGN NOTE:
Current limit is set to 500mA

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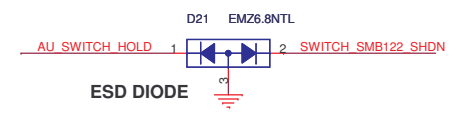
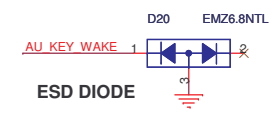
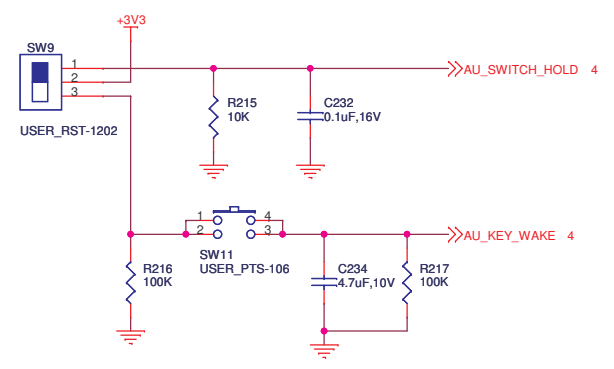
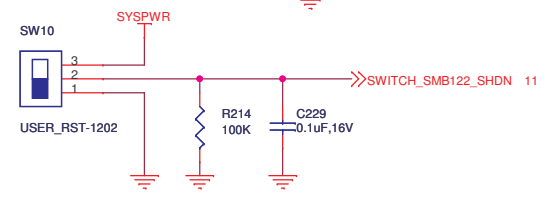
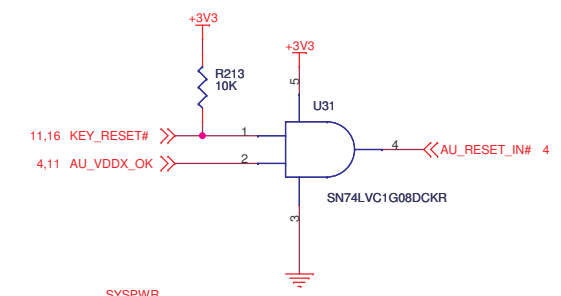
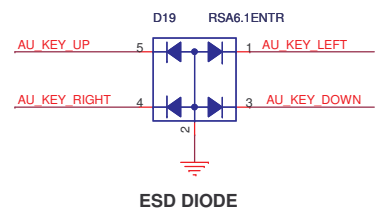
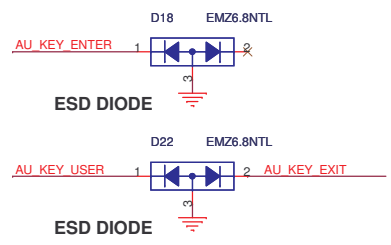
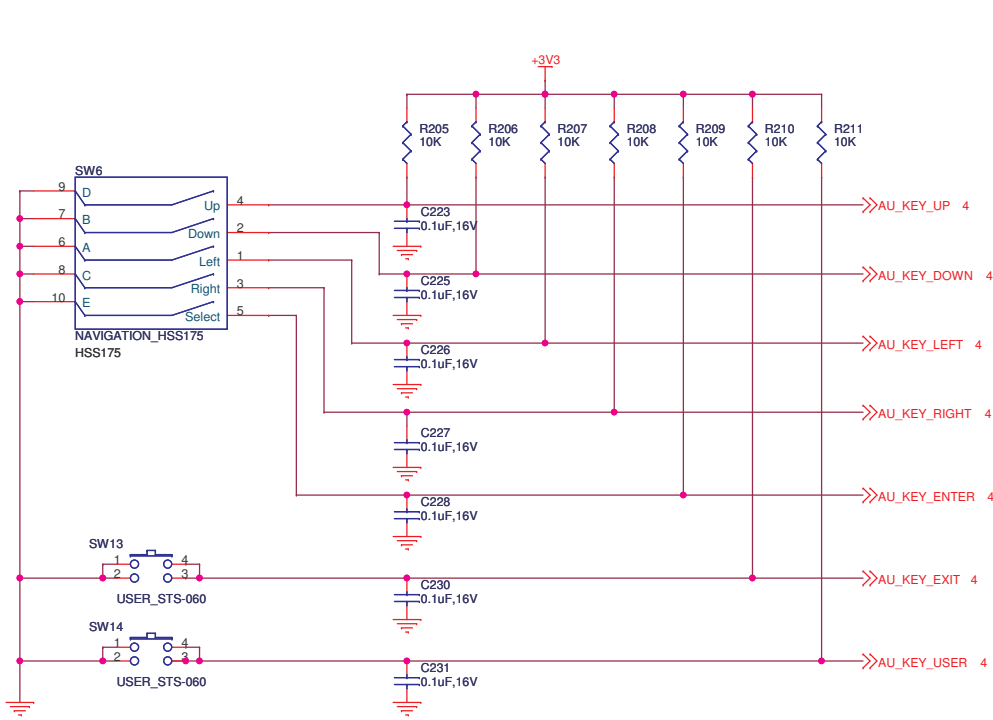
DESIGN NOTE:
Place MOSFET close to IDE connector



- 4 AU_IDE_IRO <-> AU_IDE_IRO
- 4 AU_IDE_DMARQ <-> AU_IDE_DMARQ
- 4 AU_EWAIT# <-> AU_EWAIT#
- 4 AU_HD_CS0# <-> AU_HD_CS0#
- 4 AU_HD_CS1# <-> AU_HD_CS1#
- 4 AU_IDE_IRO <-> AU_IDE_IRO
- 4 AU_IDE_DMARQ <-> AU_IDE_DMARQ
- 4 AU_EWAIT# <-> AU_EWAIT#
- 4 AU_HD_CS0# <-> AU_HD_CS0#
- 4 AU_HD_CS1# <-> AU_HD_CS1#
- 4,7,16 AU_WE# <-> AU_WE#
- 4,7,16 AU_OE# <-> AU_OE#
- 4 AU_IDE_RST# <-> AU_IDE_RST#
- 4 AU_IDE_PWR_EN# <-> AU_IDE_PWR_EN#

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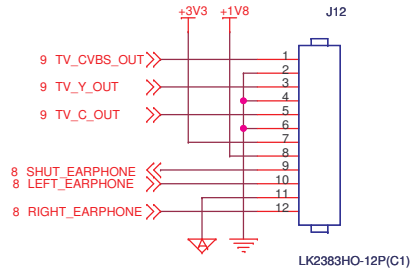
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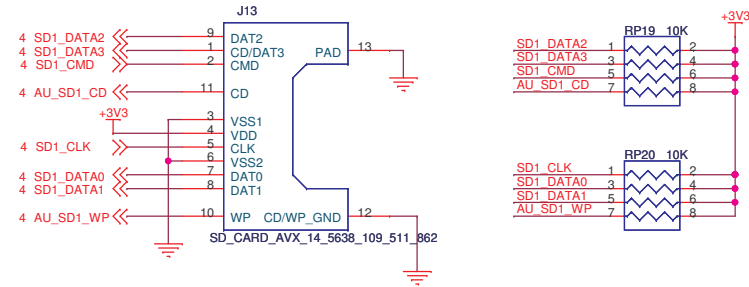
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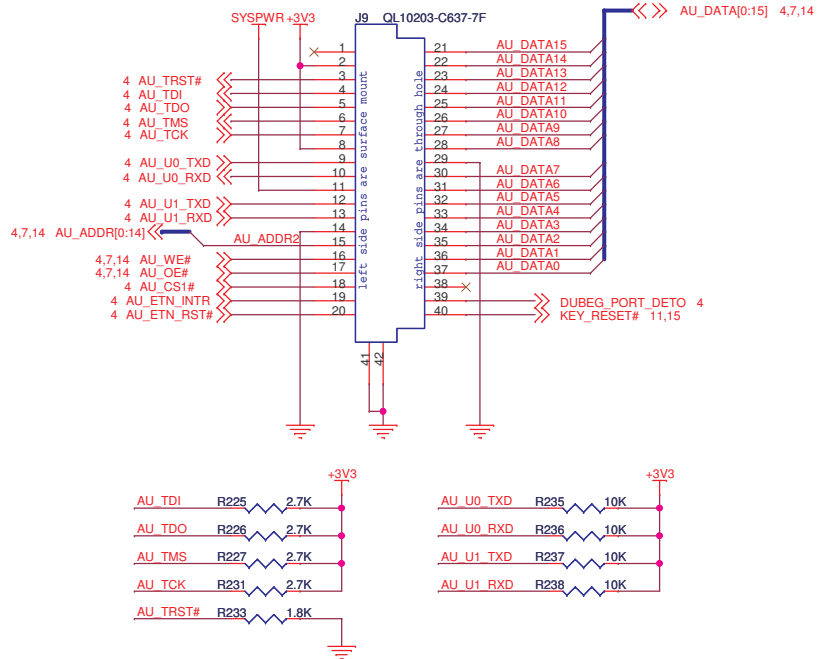
VIDEO SLOT



SD SLOT



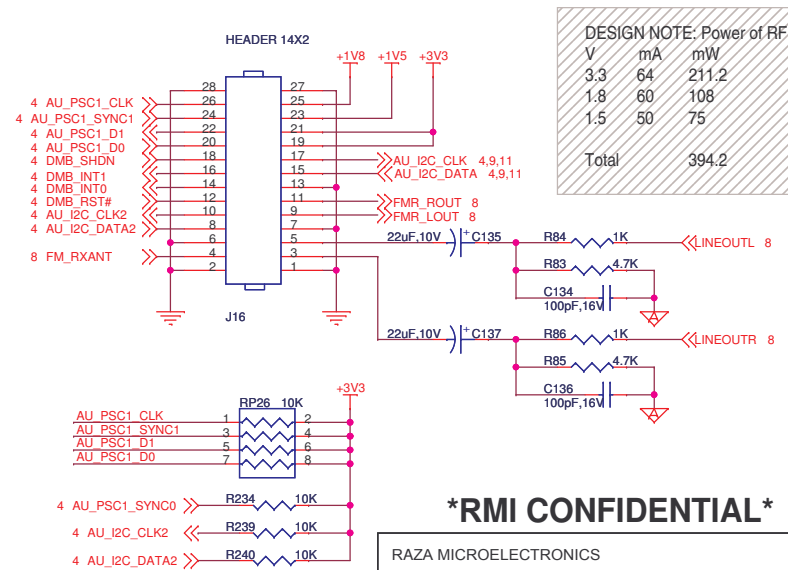
DEBUGGING SLOT



DESIGN NOTE: Signal Name

PSC Generic	SPI Specific
PSCn_CLK	SPICLK
PSCn_SYNC1	SPISEL
PSCn_SYNC0	SPISEL
PSCn_D1	SPIMISO
PSCn_D0	SPIMOSI

RF MODULE SLOT



DESIGN NOTE: Power of RF

V	mA	mW
3.3	64	211.2
1.8	60	108
1.5	50	75
Total		394.2

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GPIO ARRANGEMENT

AU_SD1_CD	GPIO_00	AU_AC97_SYNC1	GPIO_16	LCD_D0	GPIO_200
AU_SWITCH_HOLD	GPIO_01	AU_KEY_DOWN	GPIO_17	LCD_D1	GPIO_201
AU_AC97_IRQ	GPIO_02	AU_AC97_DATA0	GPIO_18	DMB_INT1	GPIO_202
AU_TVOUT_CLK	GPIO_03	AU_KEY_UP	GPIO_19	DMB_INT0	GPIO_203
AU_IDE_IRQ	GPIO_04	AU_PSC1_SYNC0	GPIO_20	DMB_SHDN	GPIO_204
AU_KEY_WAKE	GPIO_05	AU_PSC1_SYNC1	GPIO_21	DMB_RST#	GPIO_205
AU_USB_OTG_FLAG#	GPIO_06	AU_PSC1_D1	GPIO_22	AU_I2C_CLK2	GPIO_206
AU_PEN_IRQ	GPIO_07	AU_ETN_INTR	GPIO_23	AU_I2C_DATA2	GPIO_207
AU_USB_HOST_CURR_FLAG#	GPIO_08	AU_PSC1_CLK	GPIO_24	AU_I2C_CLK	GPIO_208
AU_KEY_USER	GPIO_09	AU_AC97_CLK	GPIO_25	AU_I2C_DATA	GPIO_209
AU_SMB122_DCIN	GPIO_10	AU_KEY_ENTER	GPIO_26	LCD_D8	GPIO_210
AU_PSC1_D0	GPIO_11	AU_U0_TXD	GPIO_27	LCD_D16	GPIO_211
AU_IDE_DMARQ	GPIO_12	AU_KEY_EXIT	GPIO_28	AU_SD1_WP	GPIO_212
AU_KEY_RIGHT	GPIO_13	AU_U0_RXD	GPIO_29	AU_LCD_DISP	GPIO_213
AU_KEY_LEFT	GPIO_14	AU_U1_RXD	GPIO_30	AU_CHARG_STAT	GPIO_214
AU_U1_TXD	GPIO_15	AU_AC97_DATA1	GPIO_31	AU_AC97_SYNC0	GPIO_215

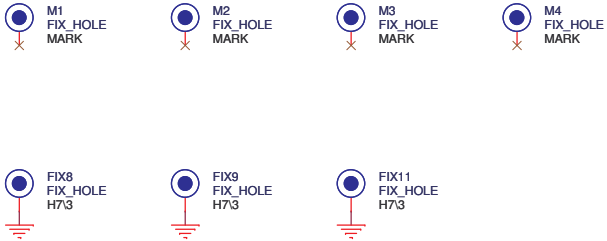
POWER CONTROL ARRANGEMENT

AU_IDE_PWR_EN#	P0.0
AU_LED_GREEN	P0.1
AU_ETN_RST	P0.2
AU_TVOUT_RST#	P0.3
AU_IDE_RST#	P0.4
AU_USB_OTG_PWR_EN	P0.5
AU_USB_HOST_PWR_EN	P0.6
AU_AMP_EN	P0.7
HP_SHUT#	P1.0
DUBEG_PORT_DETO	P1.1
RF_PER_EN	P1.2
	P1.3
	P1.4
	P1.5
	P1.6
	P1.7

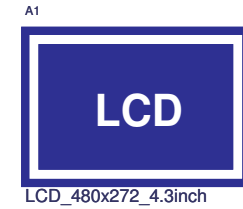
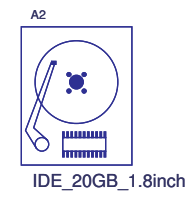
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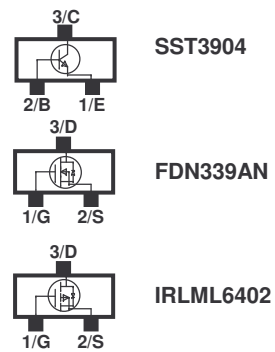
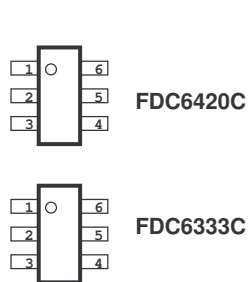
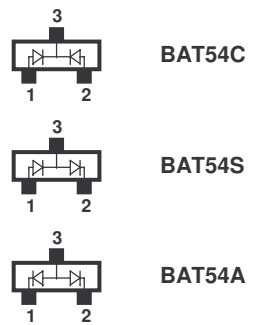
FIX HOLE



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Title RMI Alchemy Au1200 PMP Schematic			
Document Number 41103		Rev A	
Size B	Date: Wednesday, May 24, 2006	Sheet 18	of 18